PCIE mini Backplane

Clock generator & Reset fanout

File: clock_gen.kicad_sch

Direct 4-lane PCIe

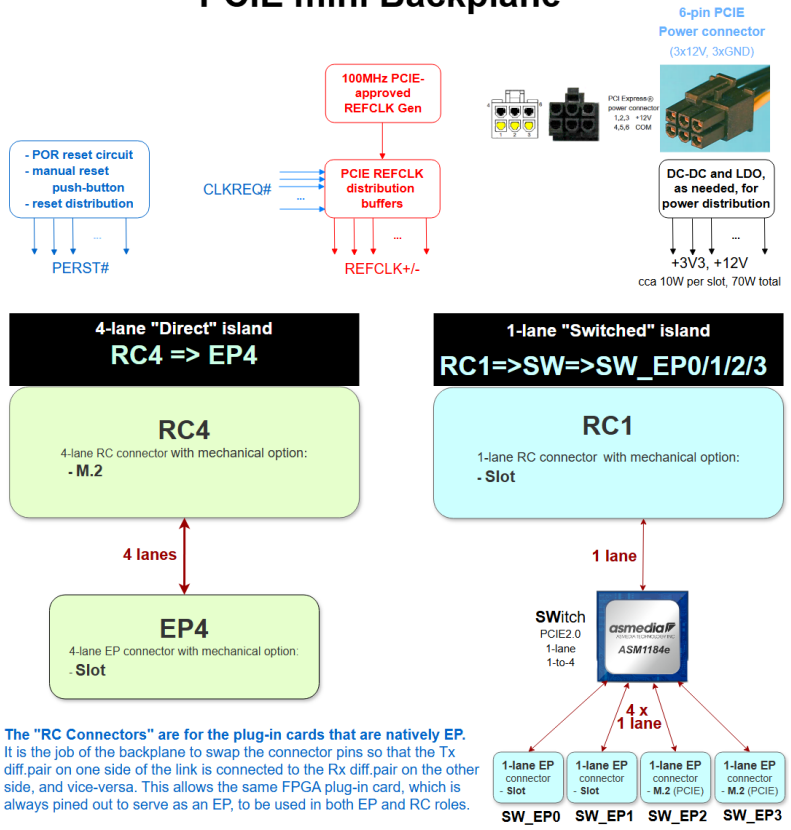
File: direct_PCIe.kicad_sch

PCIe switch

File: pcie_switch.kicad_sch

Switched 4 x 1-lanes PCIe

File: 4_1-lanes_PCIe.kicad_sch



The "RC Connectors" are for the plug-in cards that are natively EP.
It is the job of the backplane to swap the connector pins so that the Tx diff.pair on one side of the link is connected to the Rx diff.pair on the other side, and vice-versa. This allows the same FPGA plug-in card, which is always pined out to serve as an EP, to be used in both EP and RC roles.

H1 H2 H3 H4 H5 H6

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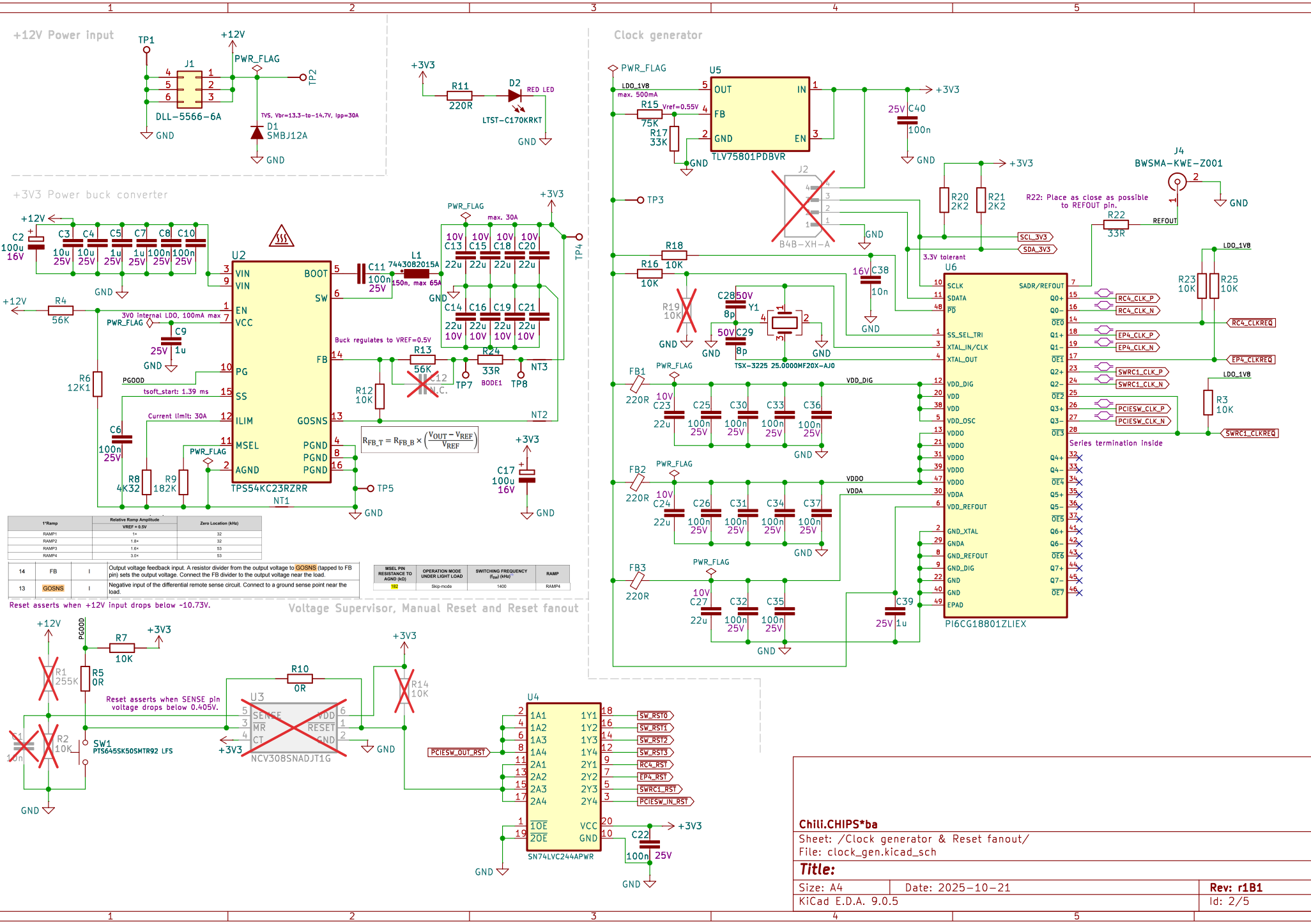
Sheet: /
File: openpci2-backplane.kicad_sch

Title:

Size: A4	Date: 2025-10-21	Rev: r1B1
KiCad E.D.A. 9.0.5		Id: 1/5



1*Ramp	Relative Ramp Amplitude VREF = 0.5V	Zero Location (kHz)
RAMP1	1×	32
RAMP2	1.8×	32
RAMP3	1.6×	53
RAMP4	3.0×	53

14	FB	I	Output voltage feedback input. A resistor divider from the output voltage to GOSNS (tapped to FB pin) sets the output voltage. Connect the FB divider to the output voltage near the load.
13	GOSNS	I	Negative input of the differential remote sense circuit. Connect to a ground sense point near the load.

MSEL PIN RESISTANCE TO AGND (kΩ)	OPERATION MODE UNDER LIGHT LOAD	SWITCHING FREQUENCY (f_{SW}) (kHz)	RAMP
182	Skip-mode	1400	RAMP4

$$R_{FB\_T} = R_{FB\_B} \times \left(\frac{V_{OUT} - V_{REF}}{V_{REF}}\right)$$

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Sheet: /Clock generator & Reset fanout/	
File: clock_gen.kicad_sch	
Title:	
Size: A4	Date: 2025-10-21
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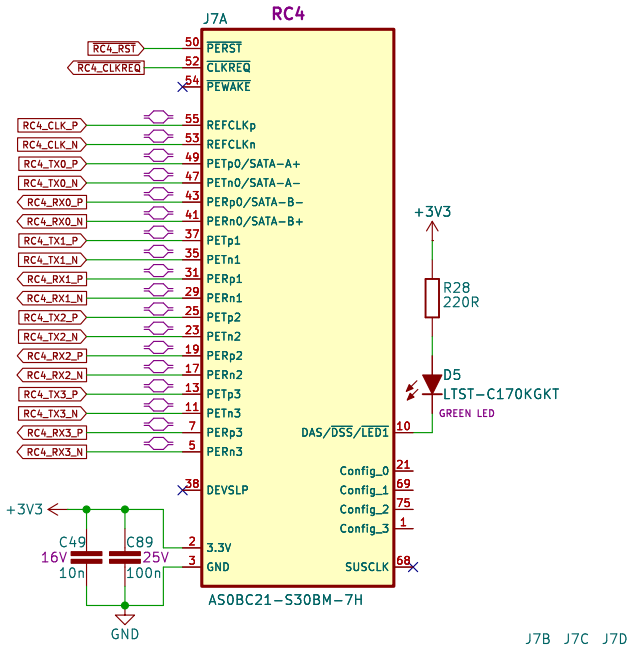
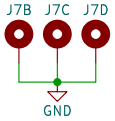
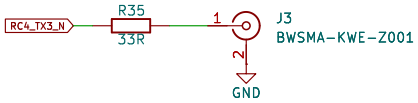
	Id: 2/5

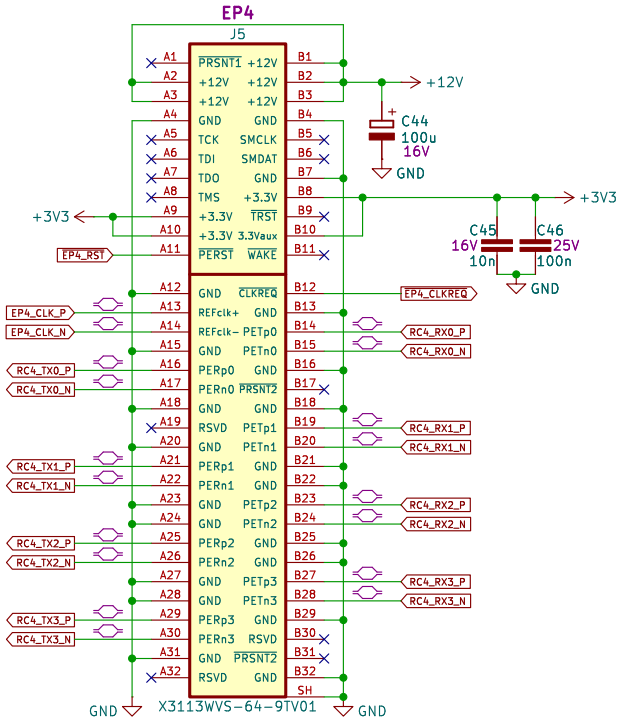
RC4

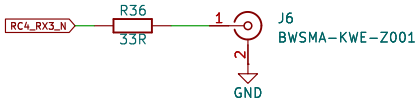






EP4





R and Connector must be placed right
next to the trace to eliminate the stub.

PCIEx1 pinout

Pin	Side B	Side A	Description
1	+12 V	~~PRSNT1#~~	Must connect to farthest PRSNT2# pin
2	+12 V	+12 V	Main power pins
3	+12 V	+12 V	
4	Ground	Ground	
5	~~SMCLK~~	~~TCK~~	SMBus and JTAG port pins
6	~~SMDAT~~	~~TDI~~	
7	Ground	~~TDO~~	
8	+3.3 V	~~TMS~~	
9	~~TRST#~~	+3.3 V	
10	+3.3 V aux	+3.3 V	Aux power & Standby power
11	~~WAKE#~~	PERST#	Link reactivation; fundamental reset [25]
	Key notch		
12	CLKREQ#[25]	Ground	Clock Request Signal
13	Ground	REFCLK+	Reference clock differential pair
14	HSOp(0)	REFCLK-	Lane 0 transmit data, + and −
15	HSOn(0)	Ground	
16	Ground	HSIp(0)	Lane 0 receive data, + and −
17	~~PRSNT2#~~	HSIn(0)	
18	Ground	Ground	
PCI Express x1 cards end at pin 18			

Legend	
Ground pin	Zero volt reference
Power pin	Supplies power to the PCIe card
Card-to-host pin	Signal from the card to the motherboard
Host-to-card pin	Signal from the motherboard to the card
Open drain	May be pulled low or sensed by multiple cards
Sense pin	Tied together on card
Reserved	Not presently used, do not connect

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Sheet: /Direct 4-lane PCIe/
File: direct_PCIe.kicad_sch

Title:

Size: A4	Date: 2025-10-21	**Rev: r1B1**
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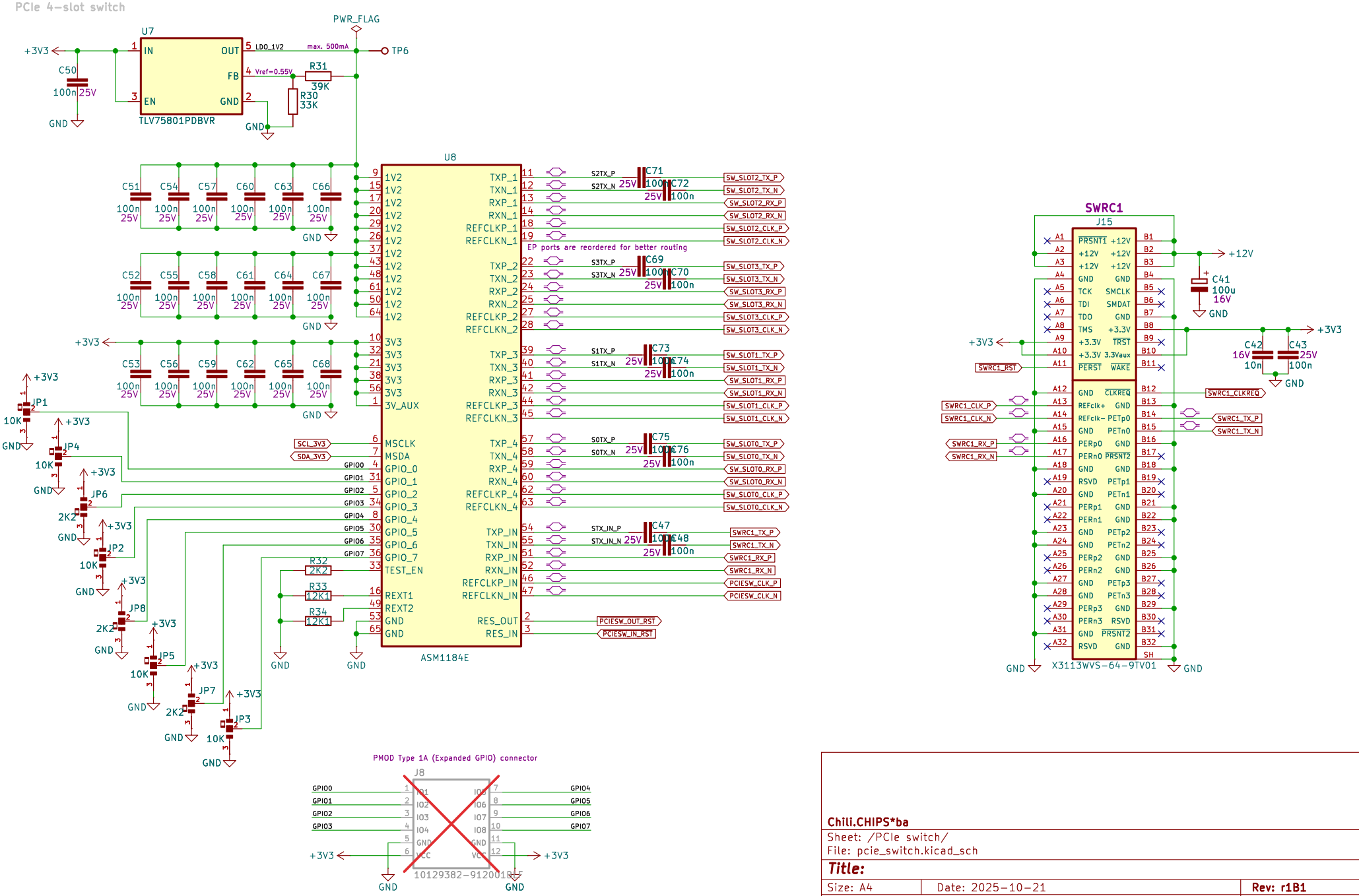
PCIe 4-slot switch



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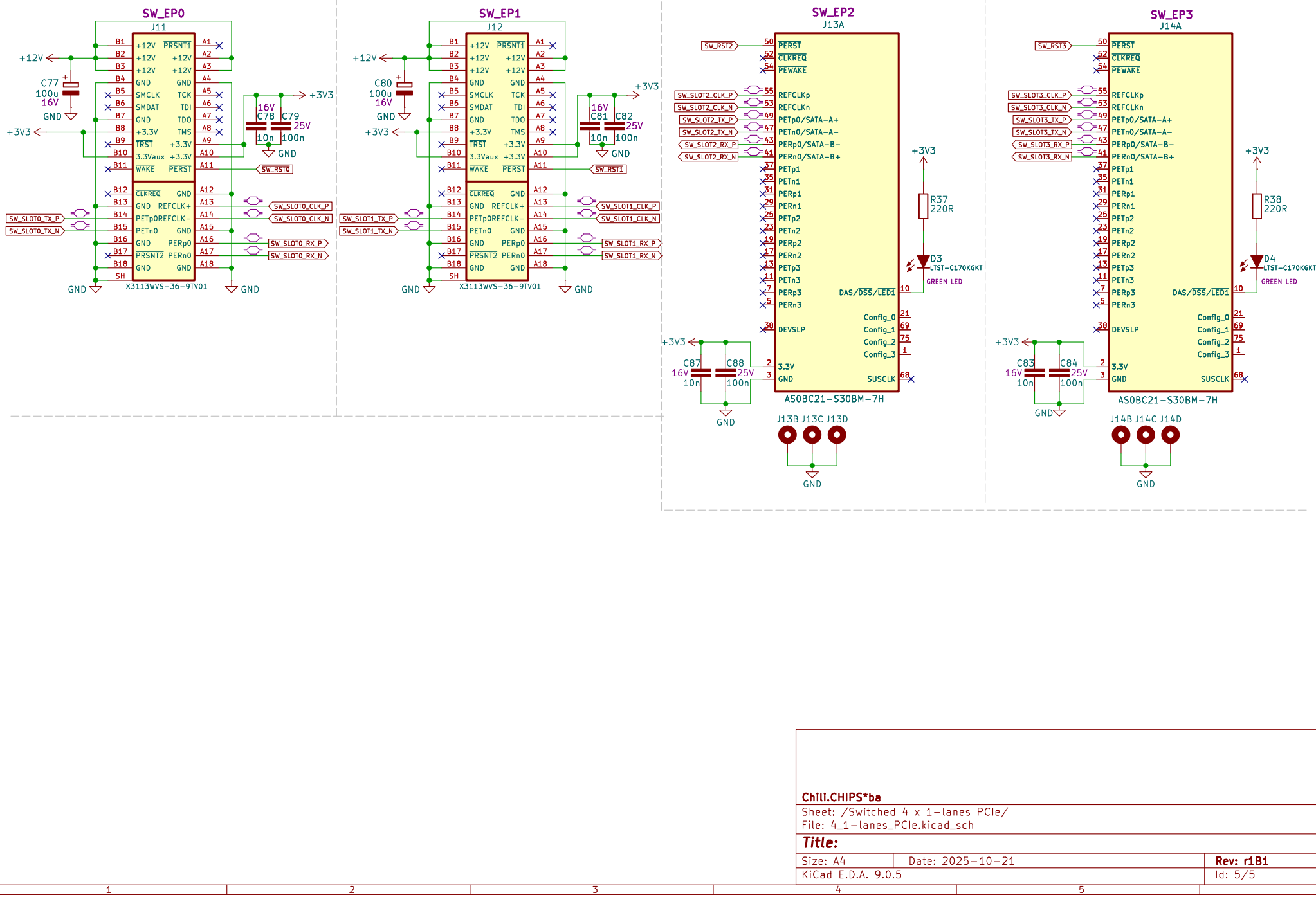
Sheet: /PCIe switch/		
File: pcie_switch.kicad_sch		
Title:		
Size: A4	Date: 2025-10-21	**Rev: r1B1**
KiCad E.D.A. 9.0.5		Id: 4/5



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Sheet: /Switched 4 x 1-lanes PCIe/
File: 4_1-lanes_PCIe.kicad_sch

Title:

Size: A4	Date: 2025-10-21	**Rev: r1B1**
KiCad E.D.A. 9.0.5		Id: 5/5