MST35885

SOM Datasheet

Revision: 1.0

Date: June 7, 2025

Content

1 Introduction

The MST35885 is a SOM equipped with octa-core Rockchip processor. It features high computing power, ultra-high efficiency and powerful hardware decoding capability. The product can be paired with high-performance motherboard to provide rich expansion interfaces, enabling it to be flexibly applied in industries such as server clusters, computer vision, commercial all-in-one display, and industrial-grade devices.

2 Features

- Equipped with a dual-cluster processor of Rockchip® RK3588, which consist of four ARM Cortex-A76 cores and four ARM Cortex-A55 cores
- Supports up to 32GB LPDDR4 and 256GB eMMC
- Supports interfaces such as I2C, USB, RJ45, PCIe, eDP, and MIPI CSI
- Features rich multi-media interfaces such as HDMI, eDP, and MIPI

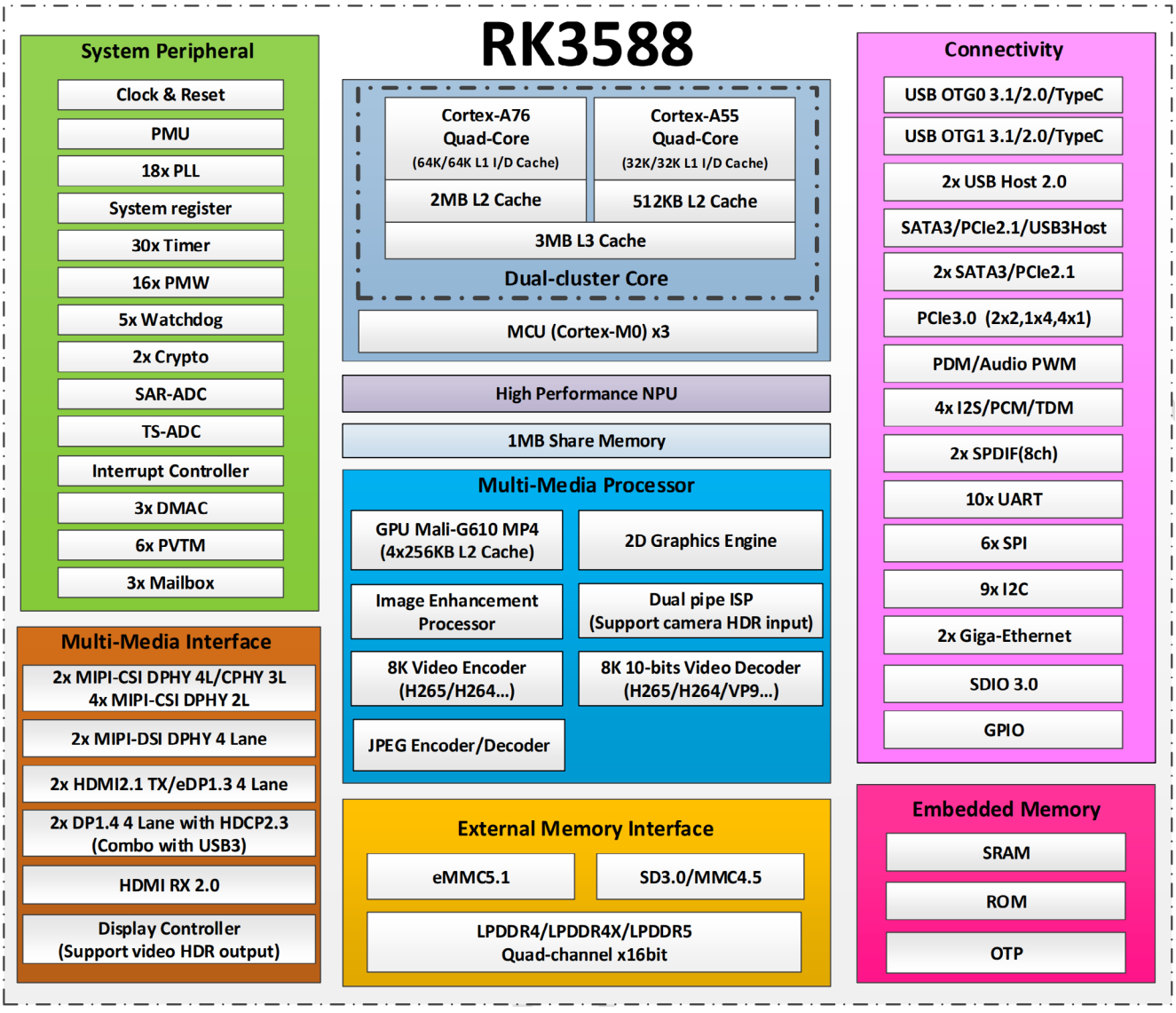
3 Applications

- Server clusters
- Computer vision
- Commercial all-in-one display
- Industrial-grade devices

4 Block Diagram

Figure 4-1 shows the block diagram of RK3588.

<Figure 4-1 Block diagram of RK3588>



5 General Specifications

<Table 5-1 General Specifications>

Parameter	Specification
Architecture	ARM
CPU	Quad-core Cortex-A76 + Quad-core Cortex-A55
GPU	ARM Mali-G610 MC4
	OpenGL ES 1.1/2.0/3.1/3.2
	Vulkan 1.1, 1.2
	OpenCL 1.1, 1.2, 2.0
OS	Android 12/ Ubuntu 20.04, supports Euler access
RAM	LPDDR4, 4GB (Up to 32GB)
Storage	eMMC, 32GB (Up to 256GB)
Display	Supports multi-screen display with a maximum resolution of 4096x2160;
	Supports dual-channel MIPI-DSI (with 4 lanes per channel) or CPHY 1.1 interface;
	Supports eDP (4K@60Hz; HDCP 2.3; DSC1.1/1.2a)
Multi-media	Supports decoding of 1080P video in multi-formats (VP9/AVS2, 8K@30fps H.264 AVC/MVC, 4K@60fpsAV1, 1080P@60fps MPEG-2/-1/VC-1/VP8);
	Supports decoding of 8K@60fps video in the format of H.2.65/ H.2.64; Supports decoding of 8K@30fps video
Connector	3*80 PIN Male Board-to-Board (BTB) connector, 1*100 PIN Male Board-to-Board connector

6 Interface Description

<Table 6-1 Interface Description>

Interface	Description
MIPI CSI x 4	Supports 2 lanes of MIPI DPHY V1.2 with a maximum data rate of 2.5Gbps per lane;
	Each 2-channel DPHY can be combined into a single 4-channel DPHY for a parallel display interface that supports up to WUXGA resolution
MIPI DSI x 2	Supports DPHY/CPHY;
	4-channel MIPI DPHY V2.0, each channel up to 4.5Gbps;
	3-channel MIPI CPHY V1.1, each channel up to 2.5Gbps
HDMI/eDP TX x 2	Supports 3.4Gbps~6Gbps HDMI2.0;
	Supports 250Mbps~3.4Gbps HDMI 1.4b;
	Supports HDCP2.3 and HDCP1.4
PCIe3.0	PCI Express Base Specification Revision 3.0 is compatible;
	Suppots dual mode of operarion: RootComplex (RC) and EndPoint (EP);
	Supports data rate: 2.5Gbps (PCIe1.1), 5Gbps (PCIe2.1), 8Gbps (PCIe3.0);
PCIE2.0	Each PCIe2.0 interface supports 1lane, data rate up to 5Gbps
USB	USB3.0 x 1, USB2.0 Host x 2, USB2.0 OTG x 2
SATA	Supports eSATA;
	Each SATA interface supports 1 port;
	Supports 6Gbps data speed
UART	UART x 6;
	Supports 5-bit, 6-bit, 7-bit and 8-bit data transmission and reception;
	Supports a baud rate of 4Mbps

<Table 6-1 Interface Description (Continued)>

I2C	I2C x 5;
	Supports 7-bit and 10-bit address mode;
	Achieves 100 Kbit/s in standard mode, 400 Kbit/s in fast mode
DAC	Supports 16-bit sampling resolution; each DAC channel supports 3 combination mode
PWM	Supports 16 on-chip PWM with interrupt-based operation;
	Programmable pre-scaling operation to the bus clock and then further scaling of the embedded 32-bit timer/counter facility;
	Supports capture mode;
	Supports continuous mode or single mode
ADC	ADC x 1
	Supports 4-channel 12-bit single-ended input SAR-ADC with a sampling rate kof up to 1MS/s.
SPI	Supports 6 SPI controller (spiro-spi4); Supports 2 chip selective outputs;
	Supports serial master and serial slave mode, and the software is configurable
I2S	I2S x 2;
	Transmit and receive clocks up to 50MHz;
	Supports Time-division (TDM), Inter-IC Sound (I2C) and other similar formats;
	Supports audio reference output clock
VAD	Supports reading voice data from I2S/PDM;
	Supports amplitude detection;
	Supports Multi-Mic array data storage;
	Supports primary combination breaks

<Table 6-1 Interface Description (Continued)>

DVP	1*8/10/12/16-bits standard DVP interface, up to 150MHz;
	Supports BT.601/BT.656/BT.1120 VI interface;
	Supports pixel_clk polarity, hsync, vsync is configurable
DP1.4	Supports 2 DP-TX1.4a interface, combined with USB3.1 Gen1;
	Each interface supports 1/2/4 lanes;
	Supports 1.62Gbps, 2.7Gbps, 5.4Gbps and 8.1Gbps Serializer, up to 7680 x 4320@30Hz;
	Supports RGB/YUV (up to 10 bit) format

7 Interface Parameters

<Table 7-1 Interface Parameters>

Parameter Name	Values			Unit	Note
	Min	Typ	Max		
Serial port communication speed	-	115,200	4M	bps	N/A
SPI clock frequency	-	-	50	MHz	N/A
I2C communication speed	-	100	400	Kbps	N/A
USB3.0 transmission speed	-	-	5	Gbps	N/A
USB2.0 transmission speed	-	-	480	Mbps	N/A
PCIe2.0 communication speed	-	-	5	Gbps	N/A

8 Electrical Characteristics

8.1 Absolute Maximum Ratings

<Table 8.1-1 Absolute Maximum Ratings>

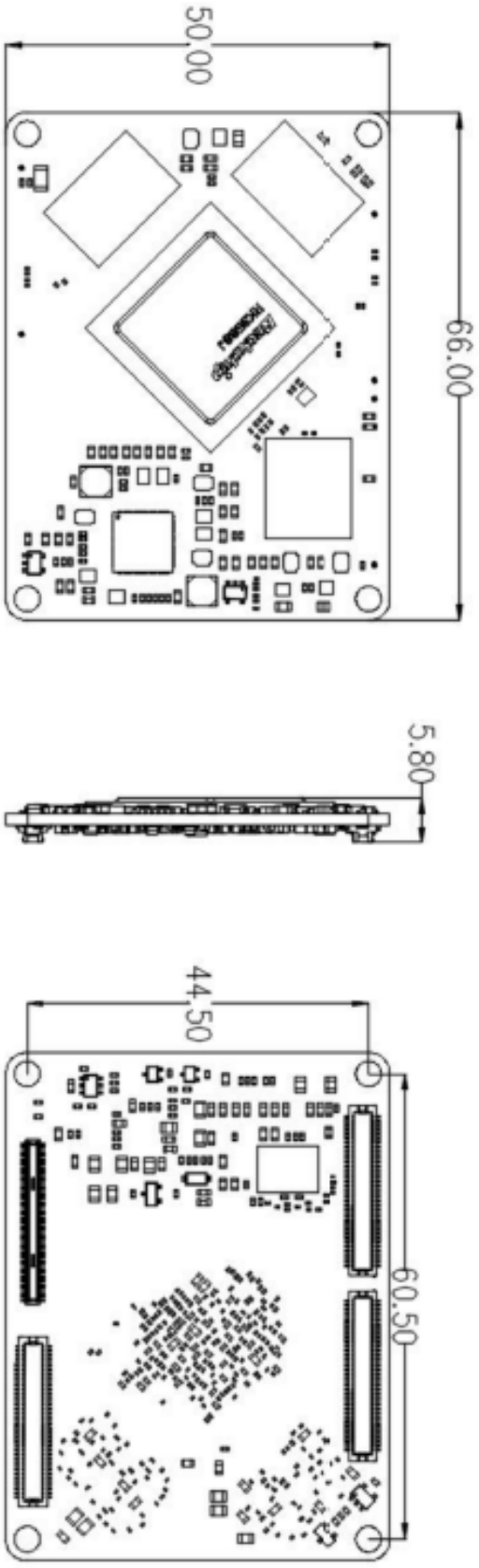
Parameter Name	Values			Unit	Remark
	Min	Typ	Max		
Input Voltage	-	4	-	V	N/A
Supply Current	-	250	3000	mA	N/A

8.2 Recommended Operating Conditions

<Table 8.2-1 Recommended Operating Conditions>

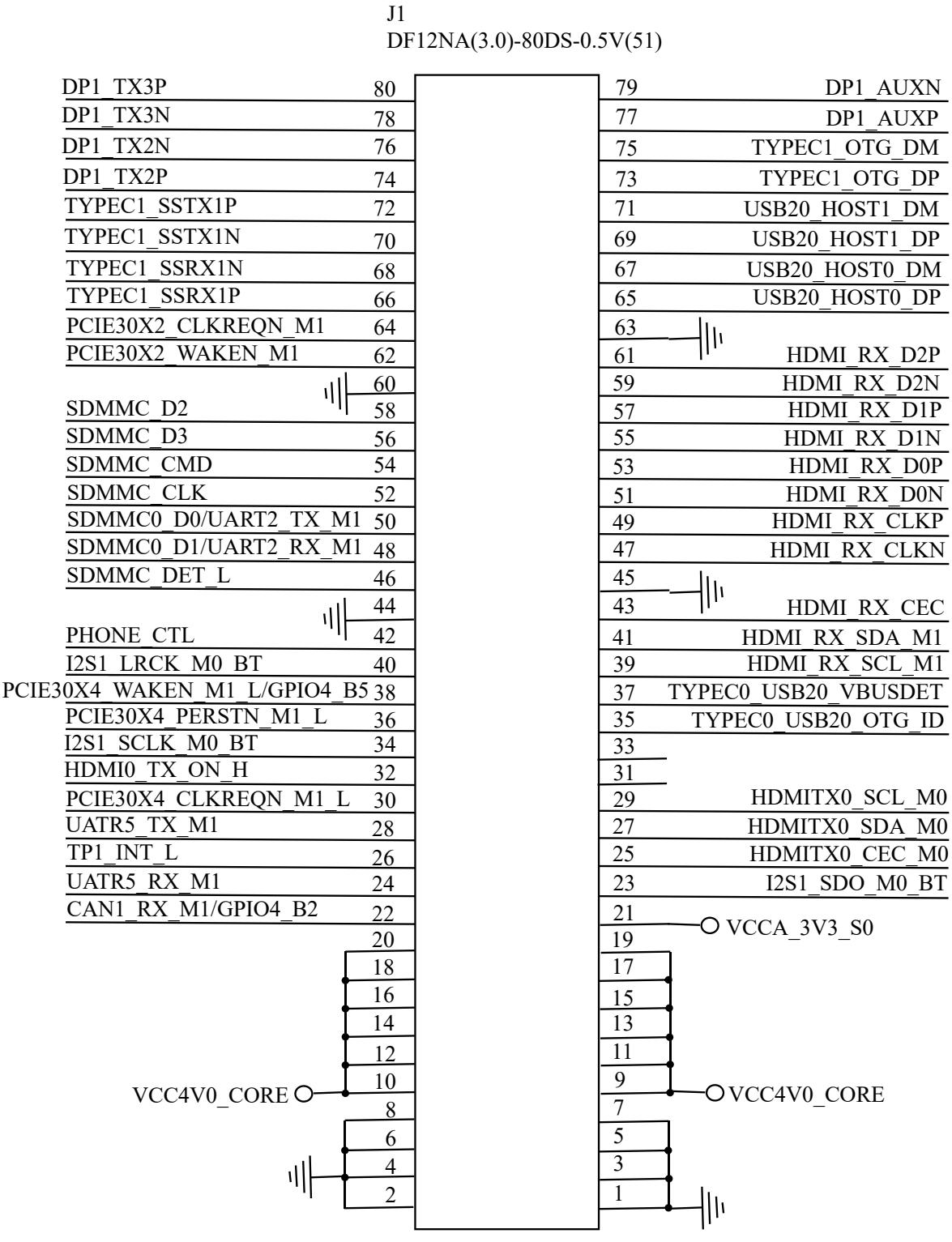
Parameter Name	Values			Unit	Remark
	Min	Typ	Max		
Operating Temperature	-40	25	85	℃	Commericial grade level
Storage Temperature	-40	25	85	℃	
Operating Humidity	10	-	90	%RH	No condensation
Storage Humidity	10	-	90	%RH	

9 Physical Dimensions

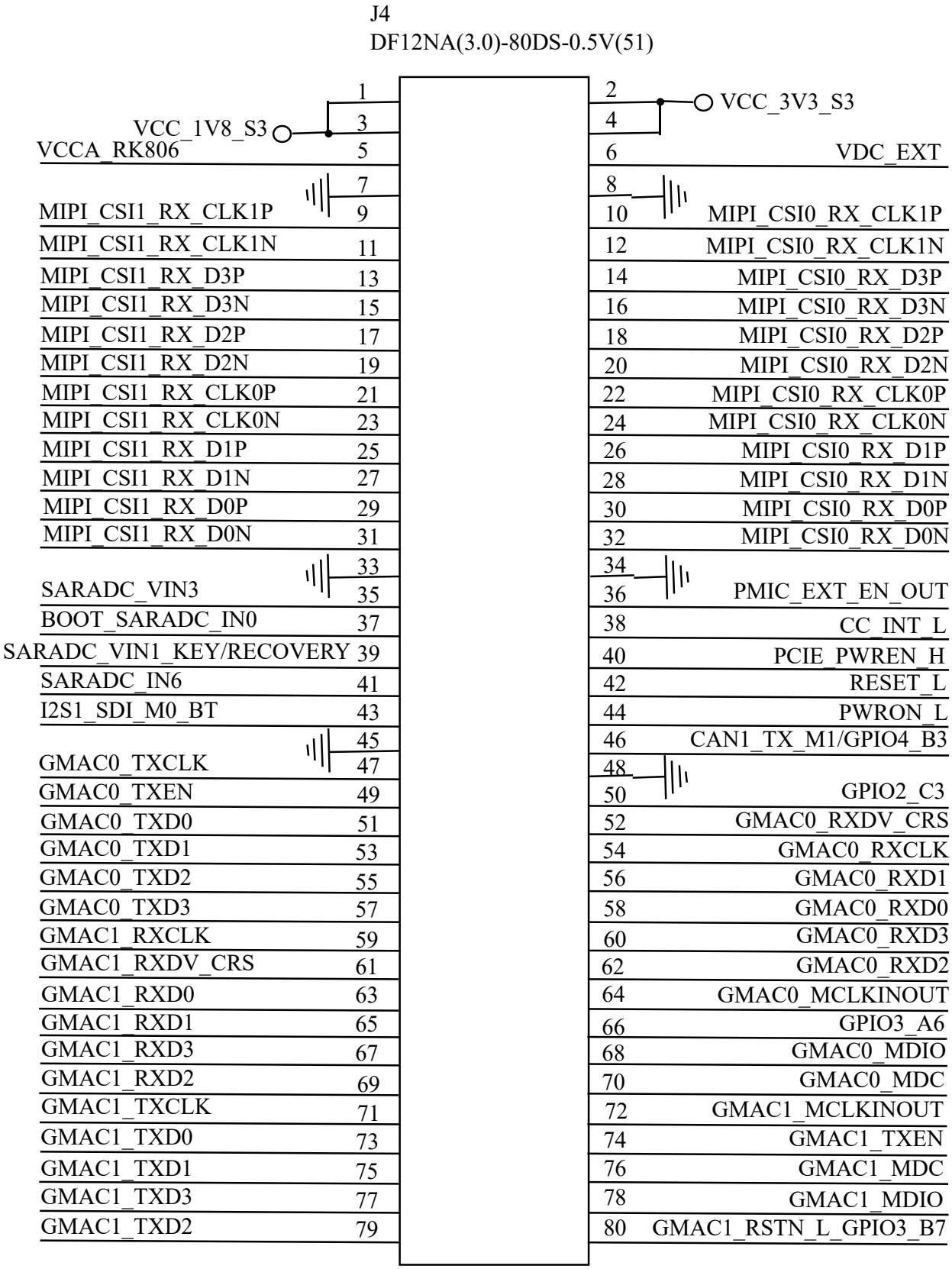


10 Connector Pinouts

<Figure 10-1 Connector Pinouts: J1 >



<Figure 10-1 Connector Pinouts: J4 >

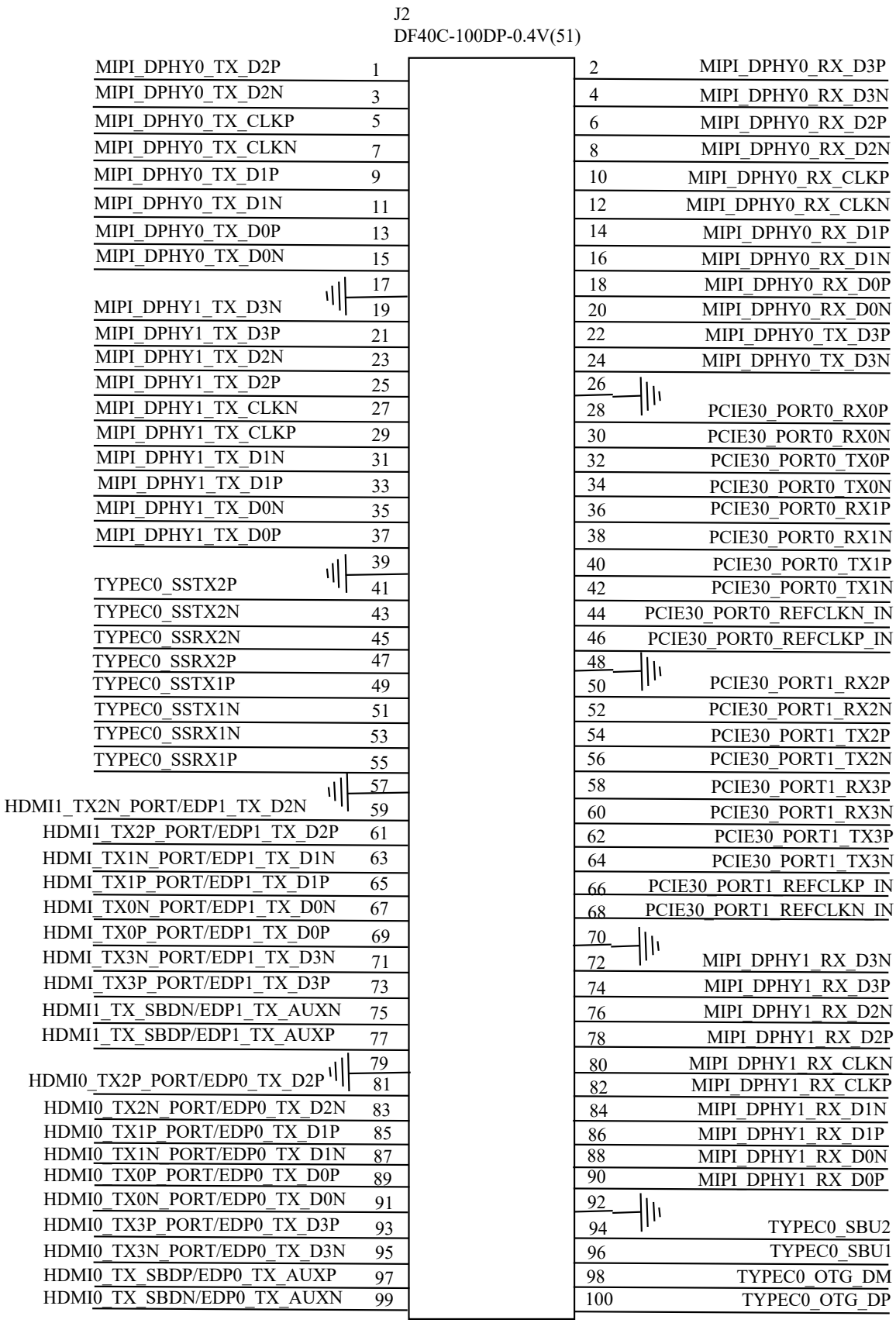


<Figure 10-1 Connector Pinouts: J3 >

J3
DF12NA(3.0)-80DS-0.5V(51)

UART0_RX_M2	2	1	
UART0_TX_M2	4	3	PCIE20_0_RXP/SATA30_0_RXP
I2C6_SDA_M0	6	5	PCIE20_0_RXN/SATA30_0_RXN
I2C6_SCL_M0	8	7	PCIE20_0_TXN/SATA30_0_TXN
GMAC1_INT/PMEB_1	10	9	PCIE20_0_TXP/SATA30_0_TXP
GMAC0_INT/PMEB_1	12	11	PCIE20_0_REFCLKP
I2C1_SDA_M2_TP	14	13	PCIE20_0_REFCLKN
I2C1_SCL_M2_TP	16	15	PCIE20_1_TXP/SATA30_1_TXP
BT_REG_ON_H	18	17	PCIE20_1_TXN/SATA30_1_TXN
TP0_INT_L	20	19	PCIE20_1_RXP/SATA30_1_RXP
HDMIIRX_HPDOUT_H	22	21	PCIE20_1_RXN/SATA30_0_RXN
I2C3_SDA_M0_MIPI	24	23	PCIE20_1_REFCLKP
I2C3_SCL_M0_MIPI	26	25	PCIE20_1_REFCLKN
UART2_RX_M0_DEBUG	28	27	PCIE20_2_RXP/SATA30_2_RXP
UART2_TX_M0_DEBUG	30	29	PCIE20_2_RXN/SATA30_2_RXN
TP0_RST_L	32	31	PCIE20_2_TXP/SATA30_2_TXP
WIFI_REG_ON_H	34	33	PCIE20_2_TXN/SATA30_2_TXN
HOST_WAKE_BT_H	36	35	PCIE20_2_REFCLKP
WIFI_WAKE_HOST_H	38	37	PCIE20_0_REFCLKN
RTC_INT_L	40	39	
BT_WAKE_HOST_H	42	41	LCD0_RESET_L
UART6_CTSN_M1_BT	44	43	I2S0_MCLK
HDMITX0_HPDIN_M0	46	45	I2S0_SDO0
UART6_RTSN_M1_BT	48	47	I2S0_SCLK_TX
VGA_HPDIN_L	50	49	I2S0_LRCK_TX
UART6_TX_M1_BT	52	51	I2S0_SDI0
UART6_RX_M1_BT	54	53	PWM15_M2
SPI1_CLK_M2/UART4_TX_M0/I2C1_SCL_M4	56	55	HP_DET_L
HDMIIRX_DET_L	58	57	I2C5_SDA_M3/UART1_RX_M1
SPI1_CS0_M2/UART4_RX_M0/I2C1_SDA_M4	60	59	I2C5_SCL_M3/UART1_TX_M1
SPI1_MOSI_M2/UART6_RX_M2/I2C7_SDA_M0	62	61	MIPI_CAM4_CLKOUT
SPI1_MISO_M2/UART6_TX_M2/I2C7_SCL_M0	64	63	MIPI_CAM3_CLKOUT
RESET0_CAM	66	65	
PCIEX1_0_WAKEN_M2_L/GPIO1_B3	68	67	DP1_HPDIN_M0
MIPI_CAM3_PWREN_H	70	69	LCD0_BL_EN_H
PCIEX1_0_CLKREQN_M2_L	72	71	GPIO2_C4
WORK_LED	74	73	MIPI_CAM4_PWREN_H
GMAC0_RSTN_L_GPIO3_C7	76	75	PWM11_M3
EDP_BL_PWM1	78	77	MIPI_CAM3_PDN_L
VCCIO5_CTL	80	79	PCIEX1_0_PERSTN_M2_L

<Figure 10-1 Connector Pinouts: J2 >



11 Revision History

Version	Date	Details
V1.0	June 7, 2025	Initial release

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